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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/817,402

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Michael I. Mandell

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27572

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09/29/2004

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EXAMINER

PHU, PHUONG M

ART UNIT

PAPER NUMBER

2631

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/817,402

Applicant(s)

MANDELL ET AL.

Examiner

Phuong Phu

Art Unit

2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 June 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-8 is/are allowed.
- 6) ☒ Claim(s) 1-4,9 and 10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>6/15/01</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation “The method of **claim 10**” on line 1. This limitation is lack of antecedent basis. It appears that the limitation should be changed to ““The method of **claim 9**”.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gou et al (5,299,192).

-As per claim 1, see figures 7A and 7B, and col. 8, line 57 to col. 11, line 59, Gou et al discloses a method (see figure 7A) comprising:

step (102, 103, 104, 105) of providing a first digital filter (102<sub>1</sub>) and a second digital filter (105<sub>a</sub>, 105<sub>b</sub>) in a subchannel (P<sup>1</sup><sub>1</sub>-P<sup>1</sup><sub>8</sub>), a first digital filter (102<sub>2</sub>) and a second digital filter

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(105<sub>c</sub>, 105<sub>d</sub>) in an adjacent subchannel ( $P^2_1$ - $P^2_2$ ), where the first and second digital filters are implemented using digital circuitry having a plurality of delay registers ( $z^{-0}, \dots, z^{-12}$ );

step (104) of adding a delay ( $z^{-2}$ ) to the second digital filters in each adjacent subchannel, such that the delay is equal to a delay greater than the delay of a delay register ( $z^{-0}$ ) in the digital circuitry; and

step (105<sub>5</sub>) of summing the two adjacent subchannels, thereby forming a composite channel (see figure 7B).

Gou et al does not disclose whether the composite channel has linear phase. He does not disclose in detail how the first and second digital filters are implemented.

However, in Gou et al system, whether or not the composite channel having linear phase would not affect the system overall performance since the condition of the composite channel having linear phase is not required (see figure 7B).

Further, implementing filters as digital filters having linear phase are well-known in the art, and the examiner takes Official Notice.

Therefore, it would have been obvious for one skilled in the art, when building or carrying out Gou et al invention, up on his design preference, to implement the first and second digital filters as filters having linear phase so that the composite channel would have linear phase without affect the system overall performance.

-As per claim 2, Gou et al discloses that the first and second filters in a cascade form (see figure 7A).

-As per claim 3, Gou et al discloses that the first and second digital filters are filters (see figure 7A).

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-As per claim 4, Gou et al discloses the first and second digital filters are implemented using techniques (see figure 7A).

-As per claim 9, see figures 7A and 7B, and col. 8, line 57 to col. 11, line 59, Gou et al discloses a method (see figure 7A) comprising:

step (102, 105) of providing a first digital filter (102<sub>1</sub>) and a second digital filter (105<sub>a</sub>) in a first subchannel ( $P^1_1$ - $P^1_4$ ), wherein the first and second digital filters are implemented in digital circuitry having a plurality of delay registers ( $z^{-0}, \dots, z^{-12}$ );

step (104<sub>a</sub>) of adding a delay ( $z^{-0}$ ) to the second filter, such that the delay is equal to the delay of a delay register ( $z^{-0}$ ) in the digital circuitry;

step (102, 105) of providing a third digital filter (102<sub>1</sub>) and a fourth digital filter (105<sub>b</sub>) in a second subchannel ( $P^1_5$ - $P^1_8$ ), where the third and fourth digital filter are implemented in the digital circuitry;

step (104<sub>b</sub>) of adding a delay ( $z^{-2}$ ) to the fourth digital filter, such that the delay is equal to an delay greater than the delay of a delay register ( $z^{-0}$ ) in the digital circuitry; and

step (105<sub>5</sub>) of summing the first and second subchannels to form a composite channel.

Gou et al does not disclose whether the first, second, third, forth digital filter and the composite channel have linear phase. He does not discloses in detail how the digital filters are implemented.

However, in Gou et al system, whether or not the first, second, third, forth digital filter and the composite channel having linear phase would not affect the system overall performance since the conditions of having linear phase are not required (see figure 7B).

Further, implementing filters as digital filters having linear phase are well-known in the art, and the examiner takes Official Notice.

Therefore, it would have been obvious for one skilled in the art, when building or carrying out Gou et al invention, up on his design preference, to implement the first and second digital filters as filters having linear phase so that the composite channel would have linear phase without affect the system overall performance.

-As per claim 10, Gou et al further discloses

step (102, 105) of providing a fifth digital filter (102<sub>2</sub>) and a sixth digital filter (105<sub>c</sub>) in a third subchannel ( $P^2_1$ ), where the fifth and sixth digital filters are implemented in the digital circuitry;

step (104<sub>c</sub>) of adding a delay ( $z^{-0}$ ) to the sixth digital filter, such that the delay is equal to the delay associated with one delay register ( $z^{-0}$ ) in the digital circuitry; and

step (105<sub>5</sub>) of summing the third subchannel with the composite channel to form a second composite.

Gou et al does not disclose whether the fifth and sixth digital filters and the second composite channel have linear phase.

However, with a similar reason set forth for claim 9, it would have been obvious for one skilled in the art, when building or carrying out Gou et al invention, to implement the fifth and sixth digital filters and the second composite channel having linear phase.

***Allowable Subject Matter***

5. Claims 5-8 are allowed.

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:30-6:00) First Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/9/04  
Phuong Phu  
Phuong Phu

**PHUONG PHU  
PRIMARY EXAMINER**

Phuong Phu  
Primary Examiner  
Art Unit 2631